REMARKS

The Office Action dated November 29, 2007 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claim 11 has been amended to more particularly point out and distinctly claim the subject matter which is the invention. Claims 1-10 and 12-23 have been allowed. No new matter has been added and no new issues are raised which require further consideration and/or search. Claim 11 is submitted for consideration.

Claim 11 was objected to because of informalities. Claim 11 has been amended to overcome the objection. Therefore, Applicant requests that the objection be withdrawn.

Claim 11 was rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,754,216 to Wong (hereinafter Wong). The rejection is traversed as being based on a reference that neither teaches nor suggests the novel combination of features clearly recited in independent claim 11.

Claim 11 recites a method for communication of rate control messages between two switches. The method includes the steps of designating a first plurality of ingress or egress ports of a first switch by a first numbering scheme. Each of the first plurality of ingress or egress ports is a unit for connecting the first switch to an external device. The method also includes designating a second plurality of ingress or egress ports of a second switch by a second numbering scheme. Each of the second plurality of ingress or egress ports is a unit for connecting the second switch to an external device. The method also

includes coupling a first link port of the first plurality of ports to a second link port of the second plurality of ports and configuring the first switch to generate a first rate control message at the first switch and relay the first rate control message to a first local communications channel of the first port. The method further includes configuring the first switch to perform a rate control function related to the second switch based on the first rate control message. The first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions based on the designations.

As outlined below, Applicant submits that the cited reference of Wong does not teach or suggest the elements of claim 11.

Wong teaches a switch fabric in communication with an Ethernet switch system. The switch fabric includes a switch processor, a memory and a FAD transceiver system for receiving and transmitting streams of cells over a high-speed data bus. The FAD transceiver includes a plurality of receive and transmit buffers, where there exists a set of buffers for every multiplex device with which the FAD is to communication. The FAD includes a logic unit, a receive buffer, a unicast transmit buffer and a multicast transmit buffer. The Ethernet switch system includes a plurality of multiplex devices that receive and transmit data packets from the FAD system and that are coupled to a plurality of Ethernet switches that route packets to external devices connected thereto. Col. 7, line 66-Col. 8 line 36 and Figure 3.

Wong further teaches that the switch processor communicates with the memory to obtain memory status information and to the logic unit of FAD. The switch processor

controls signals to the logic unit for controlling the transmission and reception of packets and for storage and retrieval from the memory. Col. 8, lines 48-60. Figure 4 shows the switch fabric in communication with a plurality of external devices for receiving and transmitting data. As shown in figure 4, FAD include three groups of buffers, the first group being receive buffers, the second group being unicast transmit buffers and the third group being multicast transmit buffers. Col. 9, line 53-Col. 10, line 5.

Applicants submit that Wong does not teach or suggest each of the elements recited in claim 11. Claim 11, in part, recites designating a first plurality of ingress or egress ports of a first switch by a first numbering scheme, each of the first plurality of ingress or egress ports being a unit for connecting the first switch to an external device. Claim 11 also recites designating a second plurality of ingress or egress ports of a second switch by a second numbering scheme, each of the second plurality of ingress or egress ports being a unit for connecting the second switch to an external device, wherein the first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions. Wong does not teach or suggest these features.

The Office Action alleges that the first plurality of ports of the present invention is equivalent to the FAD buffers that are part of switch fabric 300 of Wong. As presented in Applicants' Response filed on September 14, 2007, as is known to those skilled in the art, a port of a switch is a physical interface on a switch to which other external devices can be connected. Specifically, an ingress port is an incoming physical interface on the switch, that is, a port through which data enters the switch from an external device. An

egress port is an outgoing physical interface on the switch, that is, a port through which data leaves the switch. Therefore, each of the ingress and egress ports is unit for connecting the switch to an external device. A buffer, on the other hand, is known to those skilled in the art as a temporary storage area that interfaces with other components within the same device. While a buffer may communicate with other components, the buffer is not known to one skilled in the art as performing the same functions as an ingress or egress port.

In response to the arguments presented above, the Office Action alleged that one skilled in the art knows that a buffer can be interpreted to be an interface on a switch to which other devices can be connect. The Office Action points out that in Figure 4 of Wong, buffers 0-8 of each of FAD 414, 416 and 418 are coupled to Tap Mux devices 426-438 and communicate/interface with these devices. The Office Action further alleged that the buffers must include some type of input (ingress) interface and output (egress) interface in order to communication with the components to which they are coupled. Even if one accepts that the buffers of Wong includes ingress and egress interfaces, there is no teaching or suggestion in Wong that the ingress and egress interfaces associated with the buffers are used to connect the switch fabric with an external device. Rather, one skilled in the art would clearly understand that the ingress and egress interfaces associated with the buffers of Wong are for communication with internal components (for example a further ingress or egress port) within the switching fabric. Furthermore, one skilled in the art would clearly understand that the buffers of

Wong transmit data from the switch fabric through further egress ports on the switch fabric and that data is received on Ethernet ingress ports and further transmitted to the Tap Mux devices. In addition, as illustrated in figure 4 of Wong, the buffers receive data from the SWIP controller which receives the data from the SRAM memory. It is clearly understood that the data entered Wong's switching fabric through an ingress port that is different from the buffers. Thus, contrary to what is alleged in the Office Action, one skilled in the art would not equate the buffers of Wong with the plurality of ingress or egress ports of the present invention because they are different components that perform different functions.

Furthermore, as noted in our previous Response, Col. 12, lines 28-60 of Wong disclose that the multiplex devices of figure 4 are connected to the buffers of the FAD, on one end, and, on the other end, to port interface device chips (OctaPIDs), each of which include eight port interface device that are coupled to communicate with a plurality of different Ethernet switches. Therefore, Applicant submits that even the teachings of Wong show the difference in the functions of a port and a buffer. Therefore, Wong does not teach or suggest designating a first plurality of ingress/egress ports of a first switch by a first numbering scheme, each of the first plurality of ingress or egress ports being a unit for connecting the first switch to an external device and designating a second plurality of ingress/egress ports of a second switch by a second numbering scheme, each of the second plurality of ingress or egress ports being a unit for connecting the second switch to an external device, wherein the first plurality of ports and the second plurality of ports

are configured to perform switching and rate control functions based on the designations, as recited in claim 11.

Furthermore, Applicant submits that even if as the Office Action alleged the switching fabric of Wong is equivalent to the first plurality of ingress or egress ports of the present invention, there is no teaching or suggestion in Wong of designating a first plurality of ingress or egress ports of a first switch by a first numbering scheme, and designating a second plurality of ports of a second switch by a second numbering scheme, wherein the first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions **based on the designations**, as recited in claim 11.

In the "Response to Arguments" section, the Office Action continues to allege that because the FAD buffers of Wong are part of the switch fabric, these buffers are involved in the transmission and reception of data as well as control information between SWIP controller 414 and port interface device (OCTOPID) groups. Therefore, according to the Office Action, the buffers of Wong are configured to perform switching and rate control functions. However, there is no teaching or suggestion that the first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions **based on the designations**, as recited in claim 11. The Office Action further alleged that "it is unclear what the claimed "designations" are or how "switching and rate control function" are performed with regard to these "designations.""

Paragraph 0289 of the present application discloses that each of the ports can be given a unique numbering scheme which may be used for flow control and rate control based on the designation. Claim 11 clearly recites designating a first plurality of ingress or egress ports of a first switch by a first numbering scheme, and designating a second plurality of ports of a second switch by a second numbering scheme, wherein the first plurality of ports and the second plurality of ports are configured to perform switching and rate control functions **based on the designations.** Therefore, Applicant submits that claim 11 clearly recites the claimed "designations" are or how "switching and rate control function" are performed with regard to these "designations."

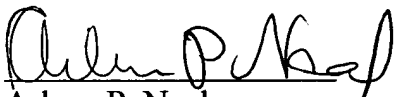
While Wong discloses that each of FAD buffers 414-418 includes multiplexers that are used to select the specific buffer that is to transmit data to the SRAM memory or that is to receive data from the SRAM, there is no teaching or suggestion that the FAD buffers of Wong are ports that are configured to perform rate switching and control functions **based the on designations**, as recited in claim 11. Therefore, Applicants respectfully assert that the rejection under 35 U.S.C. §102(e) should be withdrawn because Wong fails to teach or suggest each feature of claim 11.

As noted previously, claim 11 recite subject matter which is neither disclosed nor suggested in the prior art references cited in the Office Action. It is therefore respectfully requested that all of claim 11, in addition to claims 1-10 and 12-23, be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Arlene P. Neal
Registration No. 43,828

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

APN:ksh